WHAT IS CLAIMED IS:

1. An infrared imaging system comprising:

an infrared focal plane array comprising:

a plurality of infrared detector elements arranged in an array;

a readout circuit electrically coupled to the plurality of detector elements and comprising means for biasing the plurality of detector elements so as to provide separate detection signals corresponding to each detector element in the array, in response to incident infrared radiation and means for separately correcting offsets in the detection signals provided from the plurality of elements in the detector array to compensate for nonuniformities in the detector elements; and

output means for providing the corrected detection signals as an output of the focal plane array;

means for storing a plurality of offset correction values corresponding to the plurality of detector elements; and

means for providing the offset correction values to said means for correcting.

2. An infrared imaging system as set out in claim 1, wherein said means for correcting comprises:

a correction circuit including a plurality of parallel connected circuit elements; and

means for selectively electrically connecting said circuit elements into the detector readout circuit in response to said stored offset correction values.

3. An infrared imaging system as set out in claim 2, wherein said plurality of parallel connected circuit elements comprise a plurality of capacitors.

4. An infrared imaging system as set out in claim 2, wherein said means for selectively connecting comprises a plurality of switches, equal in number to said plurality of parallel connected circuit elements and connected in series therewith.

5. An infrared imaging system as set out in claim 1, wherein said offset correction values are binary values separately and wherein said means for storing comprises a digital memory.

6. An infrared imaging system as set out in claim 5, wherein said digital memory stores a separate binary offset correction value for each detector element in the array.

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7. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements are arranged in a plurality of rows and columns and wherein said means for correcting comprises a separate offset correction circuit for each column and wherein said means for providing said offset correction values provides said offset correction values in a time multiplexed manner to said means for correcting.

8. An infrared imaging system as set out in claim 2, wherein said plurality of parallel connected circuit elements comprise a plurality of constant current sources.

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9. An infrared imaging system as set out in claim 1, wherein said array of detector elements and said readout circuit are formed as a single monolithic integrated circuit chip.

10. An infrared imaging system as set out in claim 1, wherein said plurality of detector elements comprise microbolometer detector elements.

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11. An infrared imaging system as set out in claim 10, said wherein means for biasing comprises a constant current source coupled to said microbolometer detector elements.

12. An infrared imaging system as set out in claim 1, wherein said output means comprises one or more output buffers.

13. An infrared imaging system as set out in claim 1, wherein said focal plane array further comprises a differential amplifier with first and second inputs wherein the first input is electrically connected to the readout circuit so as to receive the detection signals and wherein the second input is connected to an adjustable reference voltage.

~~14~~ 3. An infrared imaging system as set out in claim ~~13~~ 2, wherein said capacitors have capacitances of $2^N C_0$, respectively, where C_0 is a fixed capacitance and N is a nonnegative integer.

~~15~~ 4. An infrared imaging system as set out in claim ~~14~~ 3, wherein there are four capacitors having respective capacitances of C_0, $2C_0$, $4C_0$ and $8C_0$.

~~16~~ 10. An infrared imaging system as set out in claim ~~15~~ 9, wherein said current sources provide substantially constant currents of $2^N I_0$, respectively, when coupled into said readout circuit by said means for selectively connecting, where I_0 is a fixed current value and N is a nonnegative integer.

17. An infrared imaging system as set out in claim 16, wherein there are four constant current sources providing substantially constant currents of I_0, $2I_0$, $4I_0$ and $8I_0$.

18. An infrared imaging system as set out in claim 2, further comprising timing means for providing focal plane timing signals to said readout circuit.

19. An infrared imaging system as set out in claim 18, wherein said readout circuit further comprises offset correction logic means for controlling the means for correcting in response to said timing signals provided from the timing means.

20. An infrared imaging system as set out in claim 19, wherein said offset correction logic means receives said offset correction values from said means for storing and provides them to said means for correcting in response to said timing signals.

21. An infrared imaging system as set out in claim 1, further comprising means, coupled to said output means, for analog to digital converting the corrected detection signals and providing corresponding image data for each detector element.

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22. An infrared imaging system as set out in claim 21, further comprising a memory for temporarily storing image data corresponding to all the detector elements of the array.

23. An infrared imaging system as set out in claim 1, wherein said readout circuit comprises a plurality of readout cells equal in number to the plurality of detector elements and wherein said means for correcting comprises an offset correction circuit in each readout cell of the readout circuit.

24. An infrared imaging system as set out in claim 23, wherein each offset correction circuit comprises a plurality of parallel connected circuit elements and means for selectively electrically connecting said circuit elements into the readout cell in response to the stored offset correction value corresponding to said readout cell.

25. An infrared imaging system as set out in claim 10, wherein said means for biasing comprises a fixed voltage source coupled to said microbolometers.

26. In infrared imaging system as set out in claim 25, wherein said means for correcting comprises a plurality of substantially constant current sources selectively coupled to said voltage source and in parallel with said microbolometer.

27. An infrared imaging system as set out in claim 26, wherein said means for correcting further comprises a plurality of switches coupled in series with respective constant current sources.

28. An infrared imaging system as set out in claim 27, wherein said offset correction values comprise an on or off signal supplied to each of said switches.

29. An infrared focal plane array, comprising:

a plurality of detector elements configured in a two dimensional array; and

a readout circuit electrically coupled to said plurality of detector elements and structurally integrated therewith, said readout circuit comprising:

means for biasing the detector elements so as to provide an analog detection signal from each detector element corresponding to the infrared radiation incident thereon; and

means for correcting the analog detection signal from each detector element by a discrete offset correction and providing a corrected analog detection signal, the discrete offset correction varying from detector element to detector element.

30. A focal plane array as set out in claim 29, wherein said analog detection signal is a voltage signal and the discrete offset correction comprises an offset correction voltage added to, or subtracted from, the voltage signal.

31. A focal plane array as set out in claim 30, wherein said readout circuit includes a sample and hold capacitor and wherein the detection voltage signal is provided at a sample node coupled to the sample and hold capacitor and wherein said means for correcting subtracts or adds a variable amount of charge from said sample and hold capacitor to provide a corrected voltage signal at said sample node.

32. An infrared focal plane array as set out in claim 31, wherein said means for correcting comprises a plurality of capacitors connected between said sample node and a reference voltage and a corresponding plurality of switches coupled in series with each respective capacitor and said reference voltage.

33. An infrared focal plane array as set out in claim 32, wherein said plurality of switches are selectively turned on or off to provide a desired amount of discrete offset correction for each detector element.

34. An infrared focal plane array as set out in claim 33, wherein said readout circuit further comprises means for controlling said means for correcting so as to selectively open and close said plurality of switches in a time multiplexed manner during readout of a plurality of separate detector elements.

35. An infrared focal plane array as set out in claim 33, wherein said detector elements comprise microbolometer detector elements.

36. An infrared focal plane array as set out in claim 35, wherein said means for said biasing comprises a constant current source coupled to said microbolometer detector elements and said sample and hold capacitor.

37. An infrared focal plane array as set out in claim 31, wherein said means for correcting comprises a plurality of parallel connected constant current sources connected between said sample node and reference voltage and a plurality of switches corresponding to said plurality of constant current sources and respectively coupled in series therewith.

38. An infrared focal plane array as set out in claim 31, wherein said readout circuit further comprises a differential amplifier having first and second inputs, the first input thereof coupled to said sample node and said second input thereof coupled to a adjustable voltage source.

~~39~~ 32. An infrared focal plane array as set out in claim ~~38~~ 31, wherein said readout circuit further comprises a feedback capacitor coupled between the output of the differential amplifier and said first input thereof.

~~40~~ 33. An infrared focal plane array as set out in claim ~~39~~ 32, wherein said readout circuit further comprises a switch coupled between and parallel with said feedback capacitor between the output of the differential amplifier and the first input thereof.

Sub A10 41. An infrared focal plane array as set out in claim 29 wherein said plurality of detector elements and said readout circuit are formed as a single monolithic integrated circuit wherein said readout circuit acts as a substrate for said detector elements.

42. An infrared focal plane array comprising:

a plurality of detector elements configured in a two dimensional array having a plurality of rows and a plurality of columns; and

a readout circuit coupled to said plurality of detector elements, said readout circuit comprising:

means for biasing said plurality of detector elements such that a detection signal is provided from each detector element in response to incident infrared radiation;

a single output node for each column of detector elements;

means for selectively coupling said detector elements in each column to said single output node; and

a plurality of offset correction circuits equal in number to the number of columns in said array of detector elements and respectively coupled to the output node of each said column, each said offset correction circuit including a plurality of parallel coupled circuit elements coupled between said output node and a reference node and a plurality of switches equal in number to said plurality of circuit elements and respectively coupled in series therewith so as to selectively couple selected circuit elements between said output node and reference node.

43. An infrared focal plane array as set out in the claim 42, wherein said readout circuit further comprises means for providing control signals to said plurality of switches in a time multiplexed manner, so as to control the selective opening and closing of said switches, such that differing combinations of said circuit elements may be coupled between said output node and said reference node for each detector element in a given column.

44. An infrared focal plane array as set out in claim 43, wherein said plurality of parallel connected circuit elements comprises a plurality of capacitors.

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~~46~~. An infrared focal plane array as set out in claim 43, wherein said plurality of parallel coupled circuit elements comprises a plurality of constant current sources.

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~~47~~. An infrared focal plane array as set out in claim 42, wherein said means for biasing comprises a plurality of constant current sources respectively coupled to the detector elements in each column of the array.

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48. An infrared focal plane array as set out in claim 42, further comprising a plurality of output buffers coupled to said output of each column.

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49. An infrared focal plane array as set out in claim 47, wherein said readout circuit further comprises means for controlling the time multiplexed readout of each of said output buffers.

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50. An infrared focal plane array as set out in claim 42, wherein said readout circuit further comprises a plurality of sample and hold capacitors respectively coupled to the corresponding output node of each column and wherein said output node provides the corresponding column output signal as the voltage at said node.

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51. An infrared focal plane array as set out in claim 42, wherein said readout circuit further comprises a plurality of offset switches coupled between each said column output node and the corresponding offset correction circuit so as to selectively couple said offset correction circuit to said output node.

52. An infrared focal plane array as set out in claim 42, wherein said readout circuit further comprises a plurality of differential amplifiers, each having first and second inputs and an output, the first inputs thereof being coupled to respective column output nodes and the second inputs thereof coupled to a reference voltage.

53. An infrared focal plane array as set out in claim 52, wherein said reference voltage differs between the respective differential amplifiers.

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54. A method for reading out infrared detection signals corresponding to detected infrared energy at respective detector elements of an infrared focal plane array, comprising the steps of:

biasing each detector element in the array so as to provide a separate analog detection signal from each detector element;

storing a plurality of offset correction values, corresponding to each detector element in the array;

correcting the detection signals provided from each detector element in the array using said stored offset values; and

providing the corrected detection signals as the output of the focal plane array.

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55. A method for reading out an infrared focal plane array as set out in claim 54, further comprising the step of amplifying said corrected detection signals prior to providing the signals as an output of the infrared focal plane array.

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56. A method for reading out an infrared focal plane array as set out in claim 55, further comprising the step of analog to digital converting the corrected detection signals after said amplification step.

57. A method for reading out an infrared focal plane array as set out in claim 54, wherein said correcting step comprises selectively shifting the analog signal corresponding to the detection signal from a given detector element by a discrete amount corresponding to the stored offset correction value for said detector element.

58. A method for reading out an infrared focal plane array as set out in claim 57, wherein said detection signals are voltage values provided on a sample and hold capacitor and wherein said correcting step comprises subtracting or adding a discrete amount of charge from said sample and hold capacitor.